

REMARKS

The applicant thanks the Examiner for the careful examination of this application. and respectfully requests entry of the amendments indicated hereinabove.

Claims 12-16 are pending and rejected. A new Information Disclosure Statement is enclosed herewith in response to the Examiner's rejection.

Claim 12 positively recites depositing a base polysilicon layer on the silicon substrate and defining an aperture with sidewalls; and then forming a spacer to cover the sidewalls. In addition, Claim 12 positively recites forming an emitter polysilicon layer positioned within the aperture. These advantageously claimed features are not taught or suggested by the patents granted to Chin et al., and Brighton, and the article of Walczyk et al., either alone or in combination.

Chin et al. teaches away from the advantageously claimed invention because Chin et al. specifically teaches the use of a poly plug to form the base contact after the emitter has been deposited (col. 3, line 52 through col. 4, line 10) while the Applicant teaches the formation of a poly plug as an emitter contact after the base has been formed (Claim 12). Therefore, an advantage of the Applicant's invention over the Chin et al. invention is that the Applicant's invention allows for the base link up region to be formed using a higher degree of thermal diffusion; resulting in a later formation of a shallower emitter contact with a shallower diffusion and a lower thermal budget.

Chin et al. further teaches away from the advantageously claimed invention because Chin et al. forms the sidewall spacers on the outside of the patterned emitter to form the base. Therefore, the patterned emitter will never be smaller than the lithographic capability of the equipment. Since the Applicant uses a sidewall spacer on the inside of a patterned hole in the base to define the emitter (Claim 12); the resulting emitter can be smaller than the lithographic feature size of the equipment. Since the emitter dimension (not the base dimension) forms the active area of the bipolar transistor, the Applicant's transistor will always have a smaller active device area, thereby saving wafer space and reducing power dissipation.

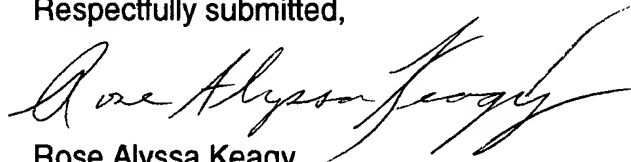
Therefore, Claim 12 is patentable over Chin et al. Furthermore, Claims 13-16 are allowable for depending on allowable independent Claim 12 and, in combination, including limitations not taught or described in the references of record.

Dependent Claims 13-15 are patentable over Chin et al. for the reasons stated above with regard to Claim 12 because claims 13-15 are dependent on allowable Claim 12. Furthermore, Claims 13-15 are patentable over Chin et al. in combination with Brighton and/or Walczyk et al. Walczyk doesn't address the advantageously claimed invention of independent Claim 12. Brighton teaches away from the advantageously claimed invention because Brighton specifically teaches the use of a poly plug to form the base contact after the emitter has been deposited (col. 4, lines 24-66) while the Applicant teaches the formation of a poly plug as an emitter contact after the base has been formed (Claim 12). Therefore, an advantage of the Applicant's invention over the Brighton invention is that the Applicant's invention allows for the base link up region to be formed using a higher degree of thermal diffusion; resulting in a later formation of a

shallower emitter contact with a shallower diffusion and a lower thermal budget. Furthermore, Brighton teaches that the base link-up diffusion must come after the formation of the emitter (col. 3, lines 58-66), thereby increasing the emitter junction depth compared to the Applicant's advantageously claimed structure.

For the reasons stated above, this application is believed to be in condition for allowance. Reexamination and reconsideration is requested.

Respectfully submitted,

A handwritten signature in cursive script, reading "Rose Alyssa Keagy".

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